REMARKS

Claims 1-26 are pending in the application. Applicants respectfully request reconsideration of the rejections set forth in the Office Action dated February 28, 2004 in light of amendments made in the previous response dated February 11, 2004 and the following remarks.

Rejections Under 35 U.S.C. §102(b)

Claims 1-24 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,812,791 ("Wasserman").

The present invention increases processing speed of motion compensation. A reference sub-region needed for motion compensation, as identified by motion information, is obtained in advance of motion compensation. According to one embodiment, the reference sub-region is stored in on-chip memory prior to motion compensation of the macroblock. Obtaining and storing multiple reference sub-regions in advance of motion compensation in this manner allows motion compensation to proceed without continuous data access delays.

As mentioned in the previous response, Wasserman fails to teach all features of the claimed invention.

The Office Action doubly uses system memory 110 in anticipation of the independent claims. This double use is not logical. Element iii) of claim 1 recites "identifying a reference sub-region based on at least the motion information", while element iv) recites "storing the reference sub-region identified by the motion information in a first memory". The Office Action uses blocks and macroblocks (coded data) to teach a reference sub-region. Wasserman stores the entire coded image data in system memory 110 (see col. 9, lines 12-17). However, the Office Action also uses system memory 110 to anticipate storing the reference sub-region identified by the motion information (see pages 2-3 and the proposed rejection for the final two claim elements). According to the Office Action then, Wasserman both finds the reference sub-region in system memory 110 and stores the reference sub-region in the same system memory 110. It is illogical for Wasserman to find data in system memory 110 and then re-store it in the same system memory. This would be a waste of memory space. And the time delays to read across a bus from external system memory 110 and re-write across the bus to the same external memory 110 further highlight illogic in the Office Action assertion. Clearly, Wasserman does not teach what the Office Action asserts and elements iii) and iv) are not taught by Wasserman.

The Office Action palpably misuses the Wasserman reference. For example, in the Response to Arguments section, the Office Action states "the reference sub-region .... is stored

in the first memory (system memory 110 of fig. 1) that is called on-chip". Where does Wasserman call system memory 110 on-chip? Quite oppositely, item 150 of Wasserman in FIG. 2 is an ASIC (Application Specific Integrated Circuit), which is usually a separate chip, and system memory 110 is unmistakably depicted outside ASIC 150 (see FIG. 2). The Response to Arguments are thus incorrect and lack support from the art of record.

For at least these reasons, it is respectfully submitted that independent claims 1, 17, 21 and 24 are not anticipated by Wasserman and are patentable.

Dependent claims 2-16, 18-20, 22-23 and 25-26 each depend directly from independent claims 1, 17 and 21 and are therefore respectfully submitted to be patentable over the art of record for at least the reasons set forth above with respect to the independent claims. Further, the dependent claims recite additional elements which when taken in the context of the claimed invention further patentably distinguish the art of record.

Withdrawal of the rejection under 35 USC §102(b) is respectfully requested.

Claims 1-2, 5-13, 17-20, and 21-24 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,084,637 ("Oku").

Similar to Wasserman, the Office Action doubly misuses memory 11 of Oku. Memory 11 is a frame buffer. According to the Office Action on page 7, Oku both a) finds the encoded data (which is stored in memory 11: see col. 9, lines 8-17), and b) stores the reference sub-region in the memory 11 (see Office Action on page 7, paragraph 2). Why would Oku find data in a memory and then re-store it in the same memory? Again, this would be a waste of memory. Memory 11 is also accessed via the command bus or data bus (see fig. 1). The time delays to read data across a bus and write back across another bus into the same memory as the Office Action asserts further highlight misuse of the reference. Thus, Oku does not teach as the Office Action asserts, and elements iii) and iv) are not anticipated by Oku.

For at least these reasons, it is respectfully submitted that independent claims 1, 17, 21 and 24 are not anticipated by Oku and are patentable.

Dependent claims 2-16, 18-20, 22-23 and 25-26 each depend directly from independent claims 1, 17 and 21 and are therefore respectfully submitted to be patentable over Oku for at least the reasons set forth above with respect to the independent claims. Further, the dependent claims recite additional elements which when taken in the context of the claimed invention further patentably distinguish the art of record. For example, Oku does not teach the limitation of claim 2: "the first memory source is an on-chip memory." Oku's system clearly employs a

memory that is coupled via a bus (see fig. 1). As is well known to those skilled in the art, such a memory is referred to as an "off-chip" memory, not an "on-chip" memory. Therefore, Oku cannot be said to teach or suggest the on-chip configuration as recited in claim 2.

Withdrawal of the rejection under 35 USC §102(b) is respectfully requested.

Applicants also note that the most recent Office Action has not remedied prior deficiencies in application of Oku. Once again, the Office Action makes no specific citations of the Oku specification to support anticipation. The broad reference to functional blocks does not clarify why Oku is relevant to the claimed features or method claims. The Response to Arguments in the Office Action dated February 28, 2004 does not remedy these deficiencies. For example, the Response to Arguments states "Oku also teach the memory (11 of fig. 1) has the same function, which stores the reference sub-regions, so the memory (11) must be on chip memory". As vague as this statement reads, memory 11 is separated by a bus and clearly not on-chip. Moreover, where does the reference teach that the memory (11) must be on chip memory?

Applicant also notes the present invention recites method claims and the Office Action has failed to mention how broad reference to functional blocks anticipates the method claims. The Office Action dated February 28, 2004 also failed to address claims added in the previous response. Claims 25 and 26 were added. Claim 25 specifically recites "wherein the first memory is an on-chip memory which forms a part of a processor, and the processor is configured to perform the motion compensation". Neither Wasserman or Oku not teach such a limitation, and Applicants respectfully request recitation in subsequent correspondence as to where the prior art of record teaches such a limitation.

Conclusion

In light of the foregoing remarks, Applicants respectfully submit that all pending claims are now in condition for allowance and respectfully request a Notice of Allowance from the Examiner. Should any unresolved issues remain, the Examiner is encouraged to contact the undersigned at the telephone number provided below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP

William J. Plut
Limited Recognition under 37 CFR § 10.9(b)

P.O. Box 778
Berkeley, CA 94704-0778
Tel: 510-843-6200, ext. 242

BEFORE THE OFFICE OF ENROLLMENT AND DISCIPLINE
UNITED STATES PATENT AND TRADEMARK OFFICE

LIMITED RECOGNITION UNDER 37 CFR § 10.9(b)

William Plut is hereby given limited recognition under 37 CFR § 10.9(b) as an employee of the Beyer Weaver & Thomas, LLP law firm to prepare and prosecute patent applications wherein the patent applicant is the client of the Beyer Weaver & Thomas, LLP law firm, and the attorney or agent of record in the applications is a registered practitioner who is a member of the Beyer Weaver & Thomas, LLP law firm. This limited recognition shall expire on the date appearing below, or when whichever of the following events first occurs prior to the date appearing below: (i) William Plut ceases to lawfully reside in the United States, (ii) William Plut's employment with the Beyer Weaver & Thomas, LLP law firm ceases or is terminated, or (iii) William Plut ceases to remain or reside in the United States on an TN visa.

This document constitutes proof of such recognition. The original of this document is on file in the Office of Enrollment and Discipline of the United States Patent and Trademark Office.

Expires: April 21, 2005

Harry I. Moatz
Director of Enrollment and Discipline